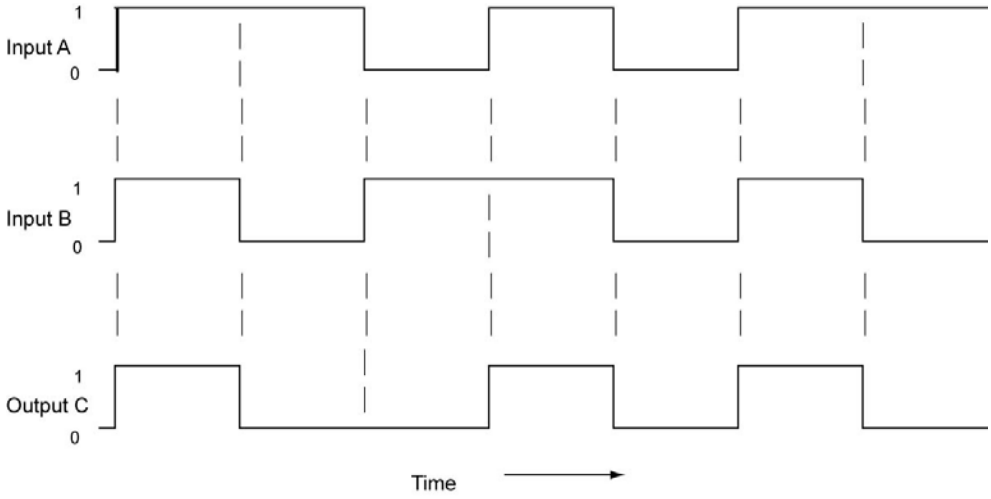
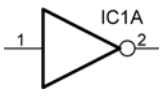
Logic Gates
Cornerstone Electronics Technology and Robotics II

- **Administration:**
  - Prayer
- **Electricity and Electronics, Sections 20.2 and 20.3, Logic Gates Continued**:
  - Timing Diagrams: Definition: A timing diagram is a graph of digital waveforms showing the actual time relationship of two or more waveforms and how each waveform changes in relation to each other.
  - Example:



Timing Diagram for Waveforms A, B, and C

  - Three Fundamental Logic Gates:
    - NOT Gates (Inverters)
    - AND Gates
    - OR Gates
    - These three basic logic gates form the basis for all digital electronic devices, that is, all digital systems; highly complex computer systems can be built entirely of these three basic functions.
  - Other Logic Gates:
    - NAND Gates
    - NOR Gates
    - XOR Gates
    - XNOR Gates
  - NOT Gates (Inverters):
    - The inverter changes the one logic level to the opposite logic level, that is, is changes a 1 to a 0 and a 0 to a 1.
    - Symbol:



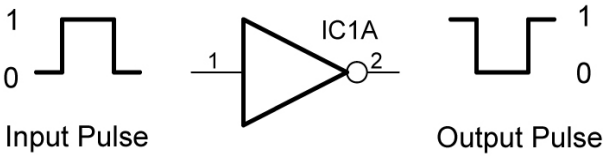
Inverter

- Truth Tables:
  - A truth table is the primary tool for displaying the logical relationships between the inputs and outputs in a digital circuit.
  - Every possible combination of inputs is listed in the columns on the left side of the truth table and the corresponding output is listed in the column on the right.
  - A truth table with N inputs has 2^N possible combinations and 2^N rows in the truth table.
  - Truth table for an inverter.

Input	Output
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)

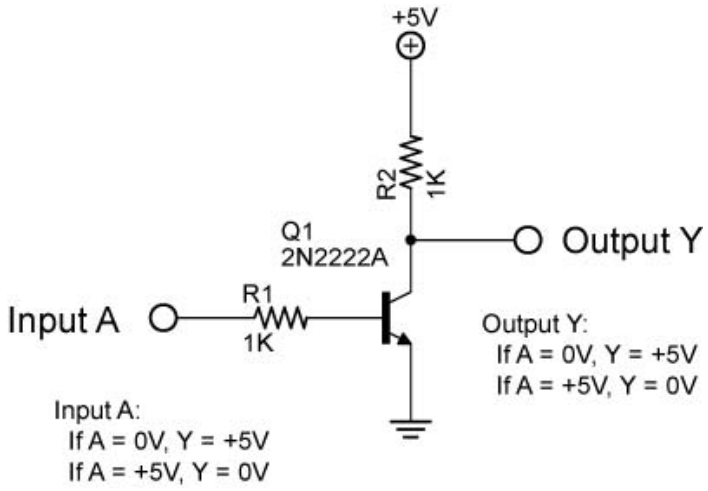
Inverter Truth Table

- Input/Output:



Input HIGH and Output LOW Pulses from an Inverter

- NPN Transistor as an inverter logic gate: The following circuit demonstrates how a NPN transistor may be wired to act as an inverter.

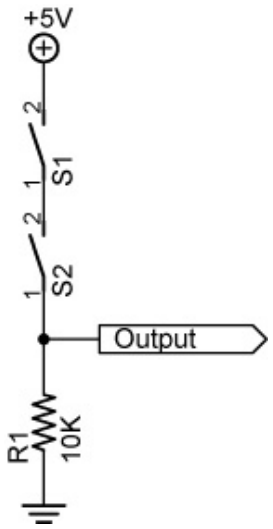


NPN Transistor Used as an Inverter or NOT Gate

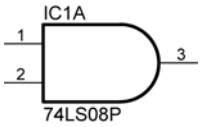
- When Input A is at 0V, the transistor base-emitter diode is reversed biased turning the transistor off. This is equivalent to an open switch between the emitter and the collector which causes Output Y to +5V.
- When Input A is at +5V, the transistor base-emitter diode is forward biased turning the transistor on. This is equivalent to a closed switch between the emitter and the collector which forces Output Y to same potential as ground, 0V.

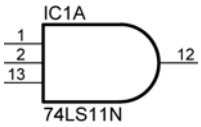
▪ See: http://elm.eeng.dcu.ie/~digital1/afdez/JavaScript/Page2.htm
▪ Perform Logic Gates LAB 1 – NOT Gates (Inverters)
▪ Do Question 1 on Class Interrupt sheet.
▪ Perform Logic Gates LAB 2 – Inverters as a Bit Storage Component

o AND Gates:
▪ The AND gate outputs a HIGH only when all of the inputs are HIGH.
▪ "All or nothing" feature: The output will be HIGH only if all of the inputs are HIGH, otherwise the output will be nothing or LOW (0V).
▪ The purpose of an AND gate is to determine when certain conditions are simultaneously true.
▪ "AND Gate" Using Switches:
- Switches can be configured in series to duplicate the function of an AND gate. In the circuit below, the output is HIGH only when both switches are closed (a 1 condition). If either or both of the switches is opened (a 0 condition), then the output goes LOW.



- AND Gate Symbol:





2-Input AND Gate **3-Input AND Gate**

- AND Gate Truth Tables:

Inputs		Output
A	**B**	
0	0	0
0	1	0
1	0	0
1	1	1

HIGH=1, LOW=0

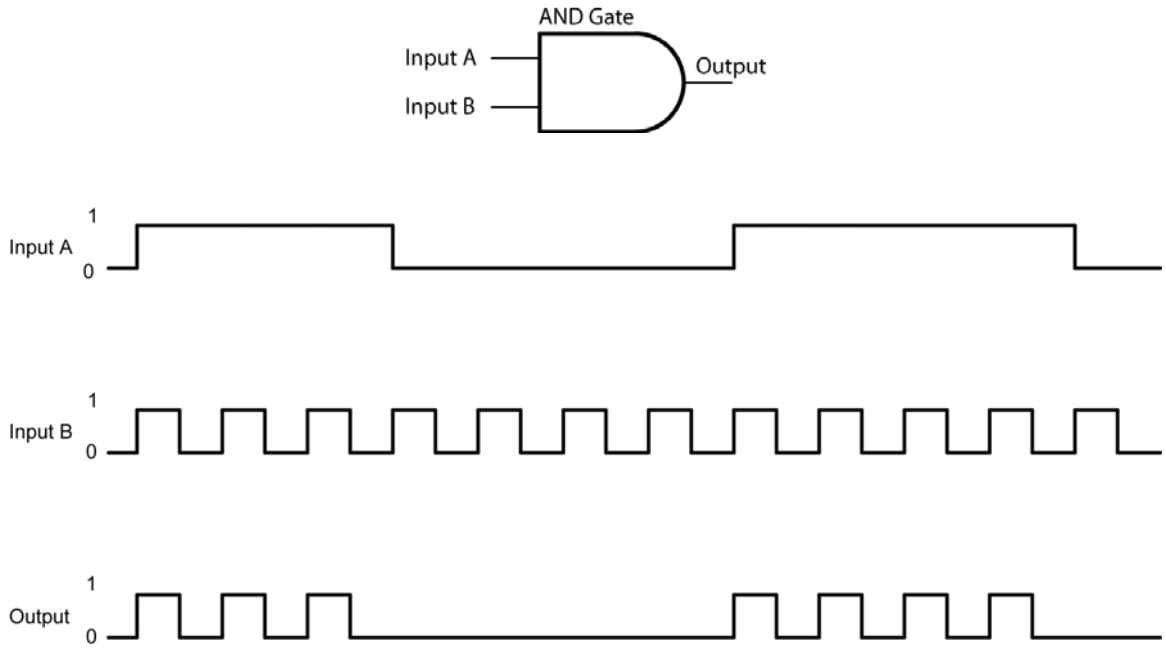
2-Input (A, B) AND Gate Truth Table

Inputs			Output
A	**B**	**C**	
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3-Input (A,B,C) AND Gate Truth Table

- See: http://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/10-gates/00-gates/and.html

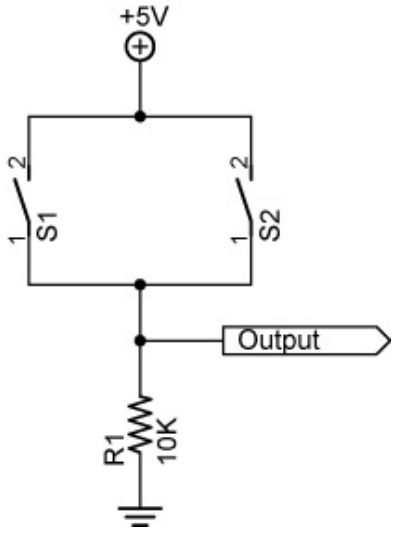
- AND gate as a data valve:
    - One of the AND gate inputs, A, may be used as a valve to permit data into the other input, B, to pass through to the output. See below.



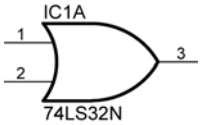
Timing Diagram Illustrating AND Gate as a Valve

    - Data into input B is only allowed to pass to the output when input A is HIGH.
- Do Question 2 on Class Interrupt sheet.
- Complete LAB 3 – AND Gates
- Complete LAB 4 – AND Gates and NOT Gates

- OR Gate:
  - "Anything" feature
  - An OR gate outputs a HIGH when <u>any</u> of the inputs are HIGH.
  - "OR Gate" Using Switches:
    - Switches can be configured in parallel to duplicate the function of an OR gate. In the circuit below, the output is HIGH if either or both of the switches is closed (a 1 condition). If both of the switches are opened (a 0 condition), then the output goes LOW.



  - OR Gate Symbol:



2-Input OR Gate

  - OR Gate Truth Table:

Inputs		Output
A	**B**	
0	0	0
0	1	1
1	0	1
1	1	1

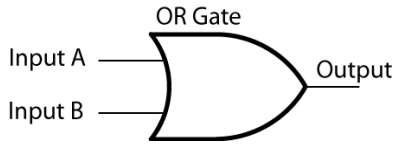
HIGH=1, LOW=0

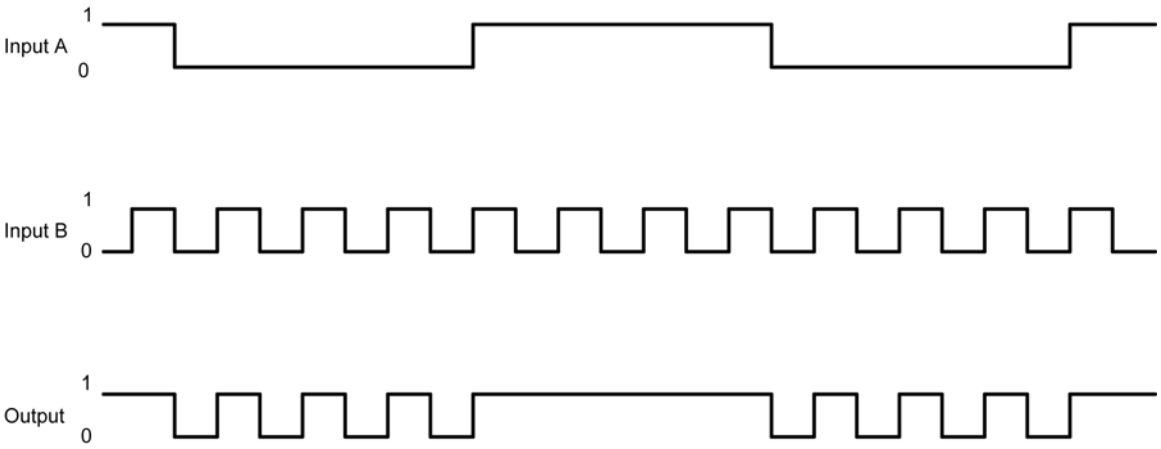
2-Input (A, B) OR Gate Truth Table

Inputs			Output
A	**B**	**C**	
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

3-Input (A,B,C) OR Gate Truth Table

- An OR gate may be used as a data valve similar to the AND gate. See below.





Timing Diagram Illustrating OR Gate as a Valve

  - Data into input B is only allowed to pass to the output when input A is LOW
- See: http://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/10-gates/00-gates/or.html
- Do Question 3 on Class Interrupt sheet.

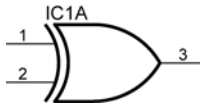
- XOR Gate (Exclusive OR Gate) Circuit:
  - XOR gates give a high output when any, but not all, inputs are high.
  - XOR Truth Table:

Inputs		Output
A	**B**	
0	0	0
0	1	1
1	0	1
1	1	0

HIGH=1, LOW=0

2-Input (A, B) XOR Gate Truth Table

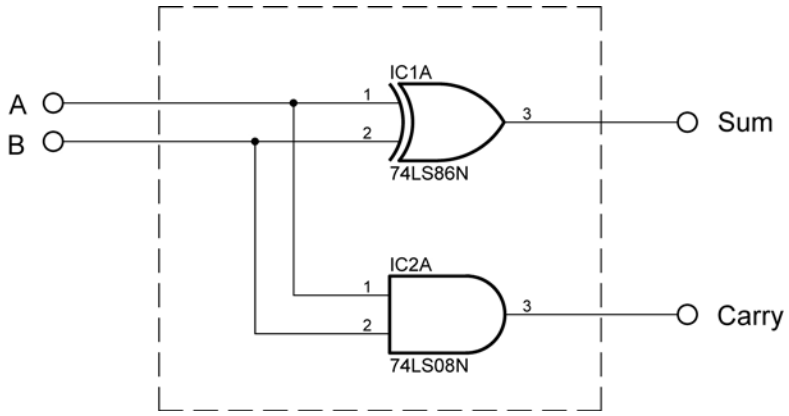
  - XOR Gate Symbol:



2-Input XOR Gate

  - See: http://www.falstad.com/circuit/e-xor.html

- Half-Adder Circuit:
  - A half-adder is a digital circuit that adds two bits and produces a sum and an output carry. It cannot handle input carries.
  - Using an AND gate and a XOR gate, we can develop a circuit that will add combinations up to 1+1.



Half-Adder

- Truth Table for Half-Adder:

Binary Inputs		Carry Output	Sum Output	Decimal
A	**B**	**(AND Output)**	**(XOR Output)**	**Equivalent**
0	0	0	0	0+0=0
0	1	0	1	0+1=1
1	0	0	1	1+0=1
1	1	1	0	1+1=2
HIGH=1, LOW=0				

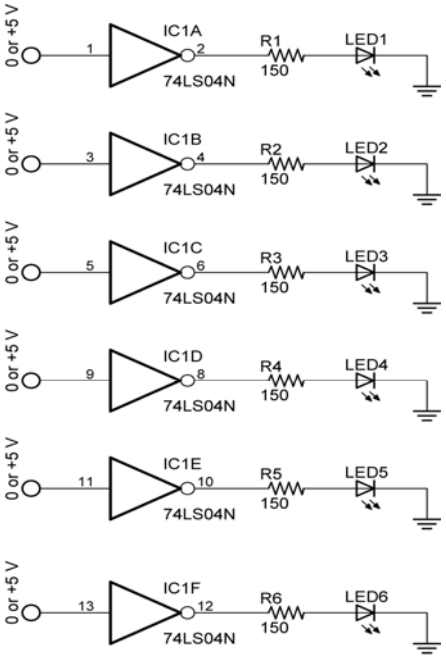
Truth Table for Half-Adder

  - To add more complicated additions, you wire a succession of circuit stages called full-adders
  - Conduct LAB 5 – Half-Adder

- See:
  - http://www.falstad.com/circuit/e-halfadd.html
  - http://www.davidviner.com/java.php?pg=3
- **Continue Building the Robotic Car:**
  - **Make sure** when mounting the motors to the motor mounts that the mounting screws **are not** too long so as to impact the gears in the gearhead motor.

Electronics Technology and Robotics II
Logic Gates LAB 1 – NOT Gates (Inverters)

- **Purpose:** The purpose of this lab is to acquaint the student with a Hex-Inverter
- **Materials:**
    - 1 – Analog/Digital Trainer or Breadboard
    - 1 – 74LS04N Hex-Inverter
    - 1 – 150 Ohm DIP Resistor Package (For Breadboard Only)
    - 6 – LEDs (For Breadboard Only)
- **Procedure:**
    - Wire the circuit below. See the photos on the next page.
    - Connect the six inputs to the HI/LOW toggles on the analog/digital trainer.
    - The LEDs on the analog/digital trainer may be used for LED1-LED6; R1-R6 may be eliminated in this case.



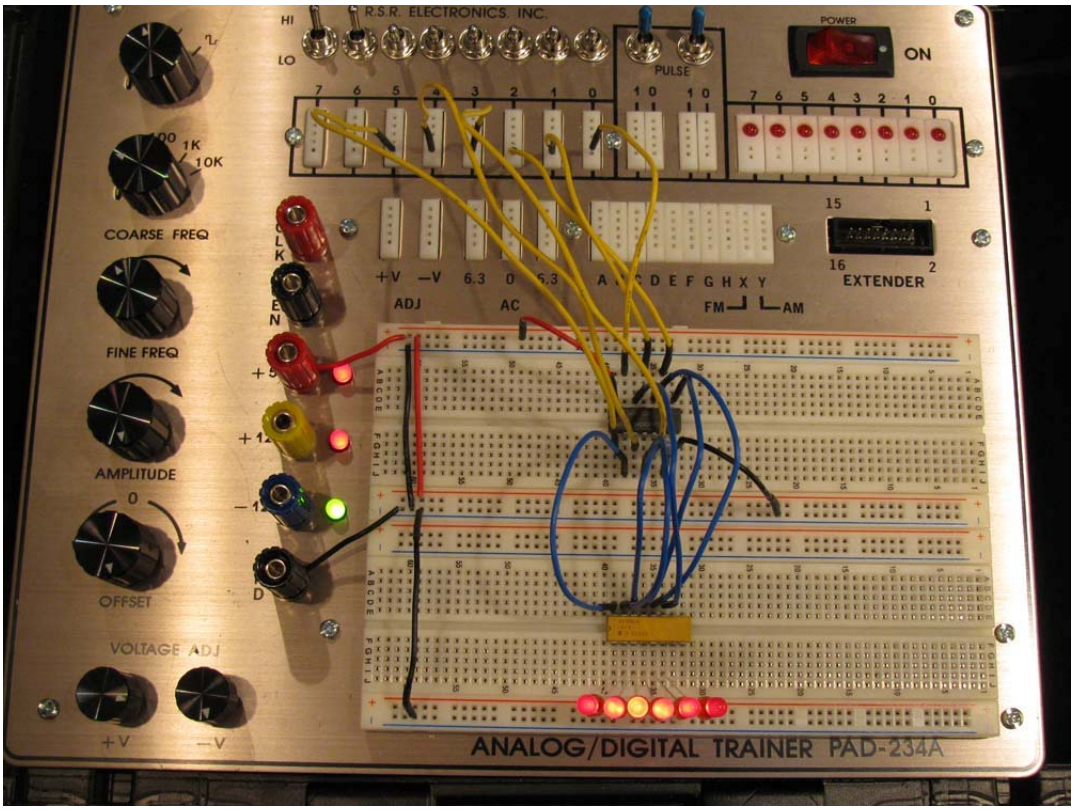
Pin 7 to Ground

Pin 14 to +5 V

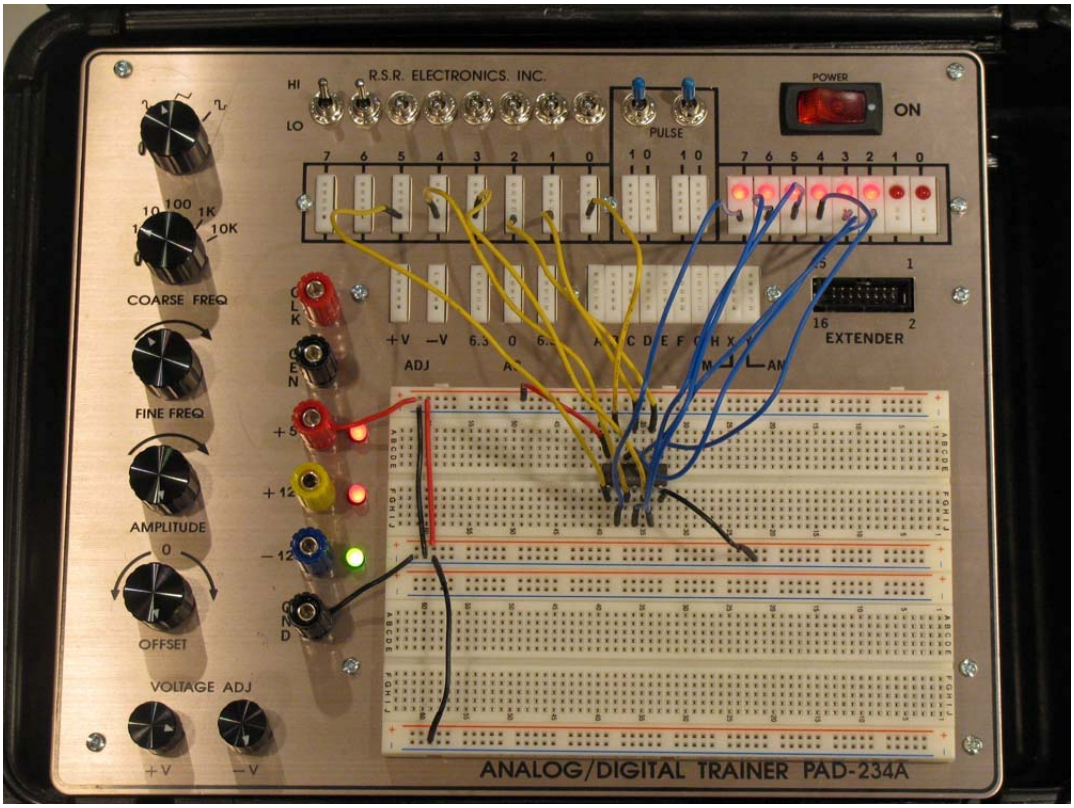
- **Results:**

Input Pin	State	Output Pin	State
1	HIGH	2	
3	LOW	4	
5	LOW	6	
9	HIGH	8	
11	HIGH	10	
13	LOW	12	

- Photo of layout on the analog/digital trainer using discrete LEDs:



- Photo of layout on the analog/digital trainer using LEDs on trainer:



Electronics Technology and Robotics II
Logic Gates LAB 2 – Inverters as a Bit Storage Unit

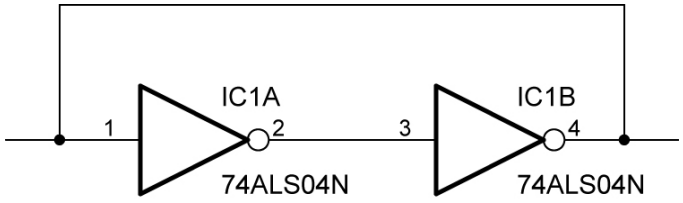
- **Purpose:** The purpose of this lab is to acquaint the student with basic bit information storage using inverters.

- **Discussion:**
  - Information (data) in digital systems must be stored for future use.
  - The basic building block for storage is in the form of a single bit (**bi**nary digi**t**).
  - The circuit below (called a flip-flop) is a simple storage unit that can store one bit of information or data (0 or +5V).
  - With eight of these bits combined, a byte is formed.

- **Materials:**

  - 1 – Analog/Digital Trainer
  - 1 – 74LS04N Hex-Inverter

- **Procedure:**
  - Wire the circuit below.
  - Connect Pin 4 to HI/LOW toggle switch and an LED.
  - Toggle Pin 4 to HIGH then disconnect Pin 4 from the toggle switch. Record the findings below.
  - Now reconnect the toggle to Pin 4 and toggle to LOW. Again disconnect Pin 4 from the toggle switch. Record the findings below.



Pin 7 to Ground, Pin 14 to +5V

Bit Storage Using Two Inverters

- **Results:**

Pin 1 & 4 HIGH	**LED on/off**	**Pin 1 & 4 Disconnected**	**LED on/off**
-		-	
Pin 1 & 4 LOW	**LED on/off**	**Pin 1 & 4 Disconnected**	**LED on/off**
-		-	

- **Conclusions:**
  - Write your conclusions based upon the results.

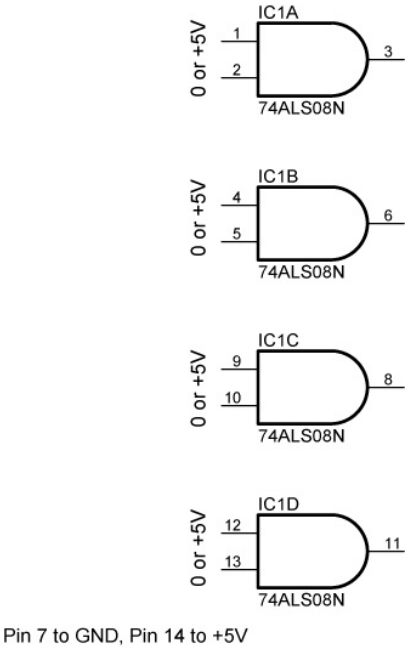
Electronics Technology and Robotics II
Logic Gates LAB 3 – AND Gates

- **Purpose:** The purpose of this lab is to challenge the student to become acquainted with the basic operation of an AND gate.

- **Materials:**

    - 1 – Analog/Digital Trainer
    - 1 – 74LS08, 2 – Input AND Gate

- **Procedure:**
    - Connect the eight inputs to the HI/LOW toggles on the analog/digital trainer.
    - Use the LEDs on the analog/digital trainer as the outputs.
    - Fill in the table in the result section.



Pin 7 to GND, Pin 14 to +5V

Quad 2-Input AND Gate

- **Results:**

Pin	HIGH/LOW
1	LOW
2	LOW
3	
4	LOW
5	HIGH
6	
9	HIGH
10	LOW
8	
12	HIGH
13	HIGH

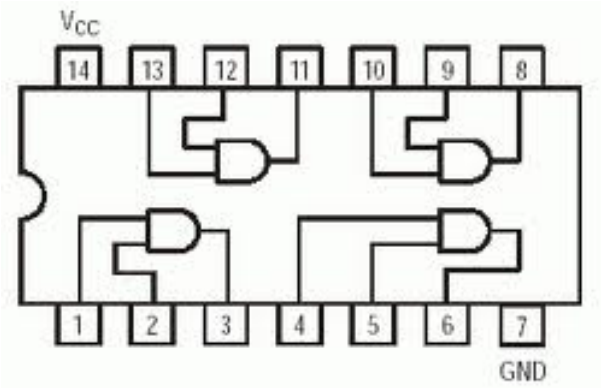
Electronics Technology and Robotics II
Logic Gates LAB 4 – AND Gates and NOT Gate

- **Purpose:** The purpose of this lab is to challenge the student to solve a real life design problem using hex-inverter (NOT gate) and an AND gate.

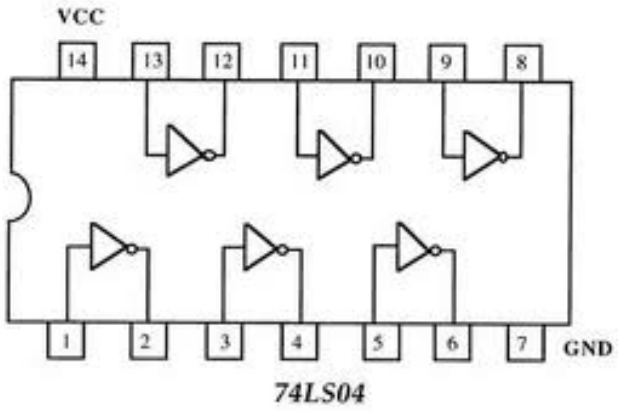
- **Materials:**

  - 1 – Analog/Digital Trainer
  - 2 – SPDT Switches (for ignition and seat belt switches)
  - 1 – 74LS08, Quad 2–Input AND Gate
  - 1 – 74LS04 Hex-Inverter (NOT Gate)
  - 1 – Piezo Buzzer

- **Procedure:**
  - Design and build a circuit using a hex-inverter and an AND gate to simulate a seat belt alarm. The alarm (piezo buzzer) must turn on only when the following two conditions are met:
    - When the ignition switch is on **and**
    - When the seat belt switch is off (the seat belt is unbuckled)
  - Use the HI/LOW toggle switches for the two switches.



74LS08 Quad 2-Input AND Gate Pinout



74LS04 Hex Inverter Pinout

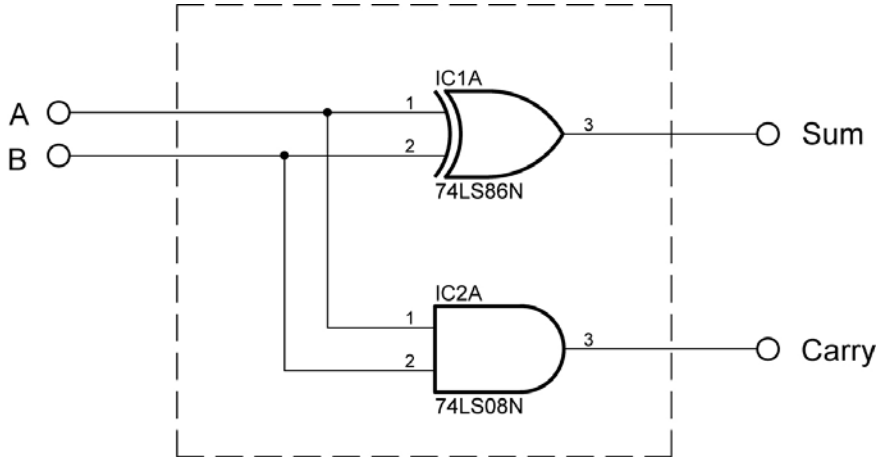
Electronics Technology and Robotics II
Logic Gates LAB 5 – Half-Adders

- **Purpose:** The purpose of this lab is to have the student connect together two logic ICs to generate a half-adder and then test their results.

- **Materials:**

  - 1 – Analog/Digital Trainer
  - 1 – 74LS06N AND Gate
  - 1 – 74LS86N XOR Gate

- **Procedure:**
  - Wire the following schematic and complete the half-added truth table.
  - Make sure not to get the chip outputs crisscrossed.
  - Verify your findings with those in the half-adder section.



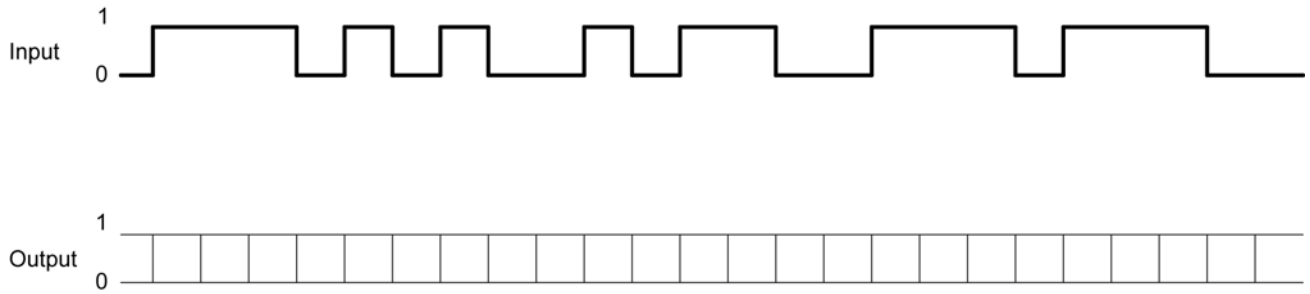
- **Results:**

Binary Inputs		Carry Output	Sum Output
A	**B**	**(AND Output)**	**(XOR Output)**
0	0		
0	1		
1	0		
1	1		

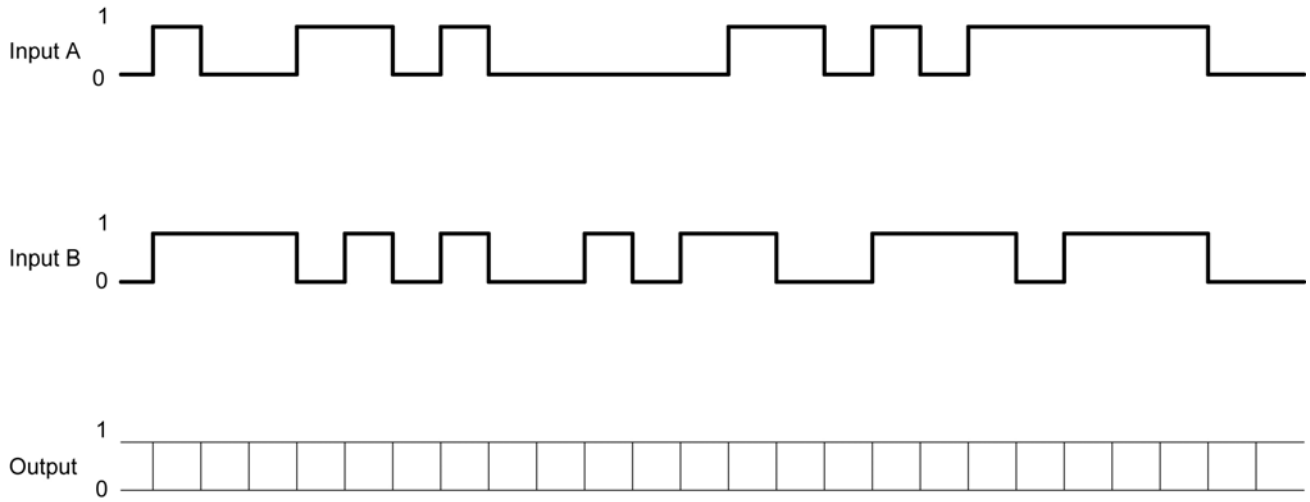
HIGH=1, LOW=0

Electricity and Electronics II, Chapter 20, Digital Circuits
Logic Gates Continued
Class Interrupts

1. Draw the output waveform for a NOT gate with the input shown below:



2. Draw the output waveform for an AND gate having the inputs shown below:



3. Draw the output waveform for an OR gate having the inputs shown below: